Understanding Size Effects in the Advanced Through-Silicon Via Interconnect Schemes for 3D ICs

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Abstract

Synchrotron X-ray microdiffraction has been successfully used to unravel how stresses evolve both in Cu through silicon via (TSV) as well as in silicon surrounding it. These findings have led to much improvements in solving the integration issues (pop-up/bulging of TSV during annealing, silicon delamination/fracture, etc.) as well as enhancing reliability and performance (reducing the "keep-away zone.") in the microelectronics devices in the last 5 years. However, today's microelectronics world has moved further into smaller and smaller technology nodes including the TSV diameters and pitches. This report will describe some of our most recent findings on the systematic studies of size effects using TSV samples fabricated with all the same fabrication methodology provided by SK Hynix, Inc. with diameters 2μm, 5μm and 8μm. Our investigation showed the smaller the TSV diameters, the stress is not necessary the smaller and thus suggested that such smaller technology could lead to further integration issues and potentially reliability and performance concerns.

Introduction

Three dimensional (3D) integrate circuit packaging technologies attract more attention because of progress in development of vertical interconnects, like through-silicon via (TSV) [1]. Despite potential benefits of TSVs in 3D packaging and integrated devices, their fabrication processes and integration still face several electrical and mechanical reliability challenges. Some of reliability issues are the result of residual thermal stress generated during manufacturing, testing, integration process steps, and operation of the TSV structures [2-3]. Stresses in the TSVs and close to active electronic devices/components are important since it can affect the electrical performance of stress-sensitive devices adjacent to the TSVs [4-5].

Stresses in Cu TSV also depend on Cu dimensions [6]. It was expected that lower diameter of TSV would have lower stresses [7]. However, the reported predictions did not take into account the microstructure of Cu TSV which may play a critical role for TSV diameters below 5μm when the Cu grain sizes become comparable with TSV diameter [1].

In this study we will investigate effect of diameter on deviatoric stresses in Cu TSV as well as surrounding silicon after fabrication and annealing using synchrotron X-ray microdiffraction (μSXRD).

Experimental Setup

Synchrotron X-ray microdiffraction has been used to measure stresses in Cu TSV. The μSXRD technique was developed at the Advanced Light Source, Berkeley Lab. The technique can provide local information about the crystal structure of materials in a microscale. This became possible due to the focusing of X-rays into a micron size spot. The analysis of the obtained X-ray diffraction patterns allow to find and quantify not only the crystal structure and lattice parameters, but also the density of geometrically necessary dislocation density, crystal bending, polygonization and rotation, and local stress/strain probing at different conditions [8]. Further details about μSXRD have been described thoroughly elsewhere [9-13]. The μSXRD experiment was conducted at the Beamline at the Advanced Light Source (ALS), Lawrence Berkeley National Laboratory (LBNL). We have studied deviatoric stress evolution in Cu TSV and surrounding silicon using μSXRD. The simplified experimental setup diagram is shown in Fig. 1(c). Incoming X-ray beam illuminate a volume that may consist of more than one crystal, the diffracted beams from each of the crystal are captured by the CCD detector placed above the sample.

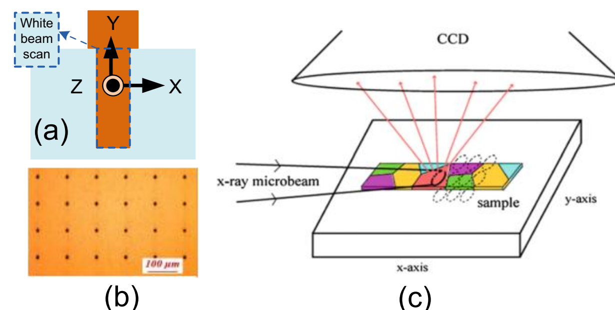

Fig. 1. Experimental setup, used to study stress in Cu TSV. (a) Cross-section view of Cu TSV showing white beam scan region and schematic of the coordinate system used to calculate deviatoric stresses. (b) Optical micrograph, showing the top view of Cu TSV sample where dark spots correspond to TSVs. (c) Experimental setup of a μSXRD. Incoming X-ray beam illuminate a volume that may consist of more than one crystal, the diffraction pattern from each of the crystal are captured by the CCD detector placed above the sample. Laue patterns are collected from each discrete volume of the sample [14].

In our experiment the white-beam (polychromatic) X-rays were used to enable measurements of deviatoric components of the stress tensor. The sample was mounted on a precision XY stage and the anode point was scanned under the focused X-ray beam as shown in Fig. 1(c). The focused X-ray beam size was 1×1μm (full-width at half-max intensity). The energy range of 5-25keV has been used for white beam X-rays. The TSV samples were fabricated with all the same fabrication

methodology provided by SK Hynix, Inc. The Cu TSVs were assembled in an array with 100μm pitch. The schematic of top view of Cu TSV is shown in Fig. 1(b). Samples were prepared by electroplating and annealed at 100°C and 400°C. After annealing the samples were polished from the top and along the cross-section to allow X-rays penetration into Cu through surrounding Si. The details of sample preparations were described in details elsewhere [5]. The white beam scan was performed over one of the TSV in each of three samples using 0.5μm step size with white beam of 1μm diameter [10]. The schematic of TSV and white beam scan region is also shown in Fig. 1(a). The deviatoric stress components of Cu TSV and surrounding silicon were studied using 2μm, 5μm and 8μm diameter of Cu TSV.

Results and Discussion

Figs. 2-7 show stress components of all deviatoric stresses (normal as well as shear) and their distribution across TSV.

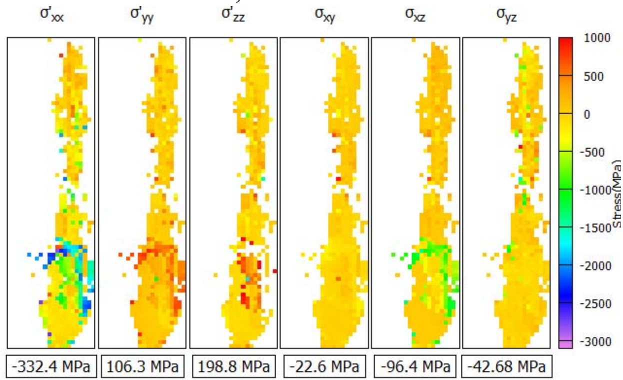

Fig. 2. White beam diffraction results for 2μm diameter of Cu TSV. The deviatoric stress in Cu after annealing at 400°C. The average stresses shown bellow each stress maps are calculated by averaging all stresses in each pixel. The pixel sizes for all stress maps are 0.5^{x}0.5μm.

The deviatoric stress distribution in 2μm diameter of Cu is illustrated on Fig. 2. The stress maps show all components of deviatoric stresses (normal and shear) and their distribution across TSV domain. The normal deviatoric stresses σ'_{xx}, σ'_{yy} and σ'_{zz} are full normal stresses (σ_{xx}, σ_{yy} and σ_{zz}) without hydrostatic components. Whereas σ_{xy}, σ_{xz} and σ_{yz} are full deviatoric shear stresses. The average of normal deviatoric stress components in 2μm diameter of Cu TSV is -9MPa, while the average shear stress component is 54MPa. The stress maps of 2μm diameter Cu TSV show that σ'_{xx} normal deviatoric stress component is highly compressive (-332MPa) while σ'_{zz} is under high tensile deviatoric stresses. When there is high normal compressive stress in σ'_{xx} direction in smaller diameter (2μm) of Cu TSV then these high compressive stresses will cause Cu TSV to expand in σ'_{yy} and σ'_{zz} direction. Which is may be one of the reason that σ'_{zz} (198.8MPa) and σ'_{yy} (106.3MPa) are higher. The deviatoric shear stress component σ_{xz} (-96MPa) is higher than σ_{xy} and σ_{yz} (-22.6MPa and -42.68). This is may be because our sample was polished in Y-direction and Z-direction which made shear deviatoric stress components of σ_{xy} and σ_{yz} more relaxed.

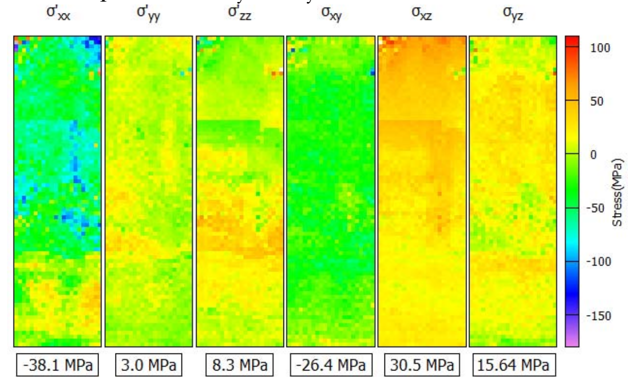

Fig. 3. White beam diffraction results for silicon surrounding 2μm diameter Cu TSV. The deviatoric stress in silicon surrounding Cu after annealing at 400°C is shown. The average stresses shown bellow each stress maps are calculated by averaging all stresses in each pixel. The pixel sizes for all stress maps are 0.5^{x}0.5μm.

The deviatoric stress distribution in silicon surrounding 2μm diameter of Cu TSV is illustrated on Fig. 3. The average normal component of the deviatoric stress is -8.9MPa, while the average shear deviatoric stress component is 6.6MPa. The average deviatoric stresses in silicon is lower than Cu. There could be couple of reasons of stresses in Cu and surrounding silicon in TSV, such as diameter of Cu TSV and coefficient of thermal mismatch (CTE) between Cu and silicon. The growth of grains in Cu TSV may be also one of reasons of high stresses in Cu. As grains grows in Cu during thermal annealing and at room temperature causing additional tensile stress in Cu [5]. High stresses in Cu TSV may cause delamination and fracture in Cu TSV. The high stresses in silicon will introduce keep-away zone and also leads to device performance and reliability issues.

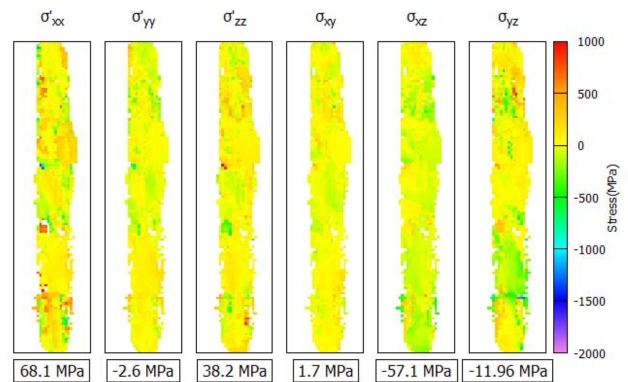

Fig. 4. White beam diffraction results for 5μm diameter of Cu TSV. The deviatoric stress in Cu after annealing at 400°C. The average stresses shown bellow each stress maps are calculated by averaging all stresses in each pixel. The pixel sizes for all stress maps are 0.5^{x}0.5μm.

The deviatoric stress distribution in 5μm diameter of Cu is illustrated on Fig. 4. The average of normal deviatoric stress components of 5μm diameter TSV is 34.6MPa which is higher than 2μm TSV sample (-9MP) but individual components of normal deviatoric stresses (σ'_{xx}, σ'_{yy} and σ'_{zz}) in 2μm diameter TSV sample are higher than 5μm diameter TSV sample. The average shear stress component 5μm is -22.5MPa whose magnitude is approximately twice lower than 2μm diameter of Cu TSV. The stress maps of 5μm diameter Cu TSV show that σ'_{yy} normal deviatoric stress component is compressive (-2.6MPa) while σ'_{xx} and σ'_{zz} (68.1MPa and 38.2MPa) are under high tensile deviatoric stresses.

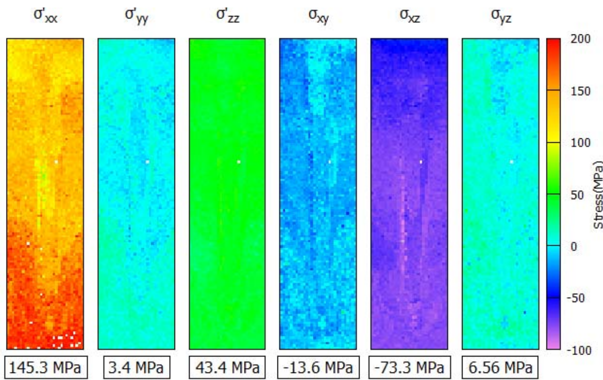

Fig. 5. White beam diffraction results for silicon surrounding 5μm diameter Cu TSV. The deviatoric stress in silicon surrounding Cu after annealing at 400°C is shown. The average stresses shown bellow each stress maps are calculated by averaging all stresses in each pixel. The pixel sizes for all stress maps are 0.5^{x}0.5μm.

The deviatoric stress distribution in silicon surrounding 5μm diameter of Cu TSV is illustrated on Fig. 5. The average normal component of the deviatoric stress is 64MPa, while the average shear stress component is -26.8MPa. For 5μm diameter Cu TSV the deviatoric normal stresses in silicon (64MPa) are higher than deviatoric normal stresses in Cu (34.6MPa). Whereas magnitude of average deviatoric shear stresses in silicon surrounding Cu TSV (-26.5MPa) are more compressive than deviatoric shear stresses in Cu TSV (-22.5MPa). The magnitude of average deviatoric normal stresses (64MPa) in silicon surrounding 5μm diameter are higher than average deviatoric normal stresses (-8.9MPa) in silicon surrounding 2μm diameter Cu TSV.

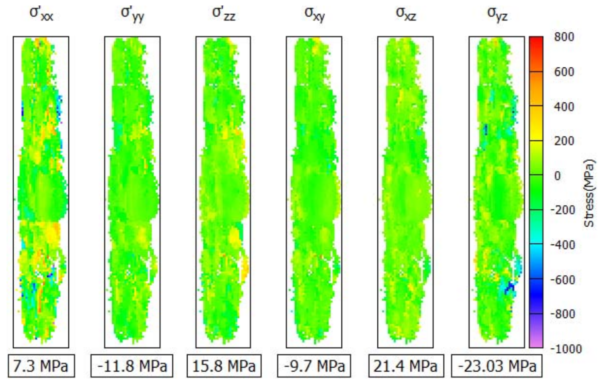

Fig. 6. White beam diffraction results for 8μm diameter of Cu TSV. The deviatoric stress in Cu after annealing at 400°C. The average stresses shown bellow each stress maps are calculated by averaging all stresses in each pixel. The pixel sizes for all stress maps are 0.5^{x}0.5μm.

The deviatoric stress distribution in 8μm diameter of Cu is illustrated on Fig. 6. The average normal component of the deviatoric stress is 3.8MPa which is lower in magnitude than 2μm sample (-9MP) and 5μm sample (34.6MPa). The average shear stress magnitude is -3.8MPa which is also lower than 2μm TSV sample (6.6MPa) and 5μm sample (-22.5MPa).

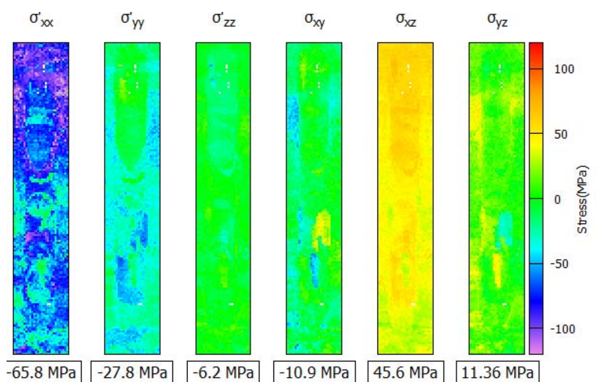

Fig. 7. White beam diffraction results for silicon surrounding 8μm diameter Cu TSV. The deviatoric stress in silicon surrounding Cu after annealing at 400°C is shown. The average stresses shown bellow each stress maps are calculated by averaging all stresses in each pixel. The pixel sizes for all stress maps are 0.5^{x}0.5μm.

The deviatoric stress distribution in silicon surrounding 8μm diameter of Cu TSV is illustrated on Fig. 7. The average normal component of the deviatoric stress is -33.3MPa, while the average shear stress component is 15.4MPa. The average magnitude of deviatoric stresses (normal as well as shear) in silicon surrounding Cu TSV of diameter 8μm are higher than in silicon surrounding Cu TSV of diameter 2μm and lower than 5μm Cu TSV. The Cu TSV diameter is also one of the factor affect stresses in silicon. Further studies are required to find more suitable diameter with less stresses.

Conclusions

Synchrotron X-ray microdiffraction has been used to unravel how stresses evolve both in Cu TSV as well as in the silicon surrounding it. These findings have led to much improvements in solving the integration issues (pop-up/bulging of TSV during annealing, silicon delamination/fracture, etc.) as well as enhancing reliability and performance (reducing the "keep-away zone.") in the microelectronics devices in the last 5 years. In this report we have described some of our most recent findings on the systematic studies of size effects using TSV samples fabricated with all the same fabrication methodology provided by SK Hynix, Inc. with three different diameters, ie. 2μm, 5μm and 8μm. Our investigation showed the smaller the TSV diameters, the stress is not necessary the smaller. Thus it is suggested that such smaller technology could lead to further integration issues and potentially reliability and performance concerns.

Acknowledgments

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