Measurement of stresses in Cu and Si around through-silicon via by synchrotron X-ray microdiffraction for 3-dimensional integrated circuits


A R T I C L E   I N F O
Article history:
Received 20 July 2011
Received in revised form 28 September 2011
Accepted 18 October 2011
Available online 17 November 2011

There is much interest recently in the 3-D interconnects using through-silicon via (TSV) technology in the microelectronics industry due to their potential for vast improvements in the performance of microelectronics devices as well as their promises in enabling advanced multi-level chips integrating diverse CMOS technologies with each other as well as with emerging technologies such as MEMS and bio-chips [1,2]. One of the key enablers for the successful implementation of 3-D interconnects using TSV is the control of the mechanical stresses in the Cu TSV itself as well as in the surrounding silicon substrate [3,4]. Stresses induced intrinsically by thermal treatment in the TSV interconnect schemes, as well as stresses induced extrinsically, for example due to silicon wafer thinning or chip-package interactions, introduce new reliability challenges for through-silicon via (TSV) technology, while stresses in the silicon substrate surrounding the copper-filled TSV can affect electron mobility in the transistors and thus determine the keep-away distance in Si was determined to be about 17 μm. Our results suggest that Cu stress may lead to reliability as well as integration issues, while Si stress may lead to device performance concerns.

A B S T R A C T
Through-silicon via (TSV) has been used for 3-dimensional integrated circuits. Mechanical stresses in Cu and Si around the TSV were measured using synchrotron X-ray microdiffraction. The hydrostatic stress in Cu TSV went from high tensile of 234 MPa in the as-fabricated state, to −196 MPa (compressive) during thermal annealing (in situ measurement), to 167 MPa in the post-annealed state. Due to this stress, the keep-away distance in Si was determined to be about 17 μm. Our results suggest that Cu stress may lead to reliability as well as integration issues, while Si stress may lead to device performance concerns.

© 2011 Elsevier Ltd. All rights reserved.
was conducted after TSV fabrication in the present study as specified further in the manuscript. The TSV test structures are of 20 \( \mu \text{m} \) diameter and 90 \( \mu \text{m} \) height and assembled in an array with 90 \( \mu \text{m} \) pitch as shown in Fig. 1.

The synchrotron X-ray microdiffraction experiment was conducted at the Beamline 12.3.2 at the Advanced Light Source (ALS), Lawrence Berkeley National Laboratory (LBNL). Both monochromatic (at 10 keV energy) as well as polychromatic (white-beam, energy scanning was conducted from 9.8 keV to 10.20 keV with 0.01 keV steps) X-rays were used to enable measurements of hydrostatic and deviatoric components, respectively, of the stress tensor. The deviatoric components of the stress tensor in the Cu TSV were studied at the post-annealed state (after annealing at 200 \( ^\circ \text{C} \) for 1 h) as well as during annealing at 200 \( ^\circ \text{C} \) using two different samples. The sample was mounted on a precision XY MICOS stage and the TSV of interest was raster scanned under the focused X-ray beam. The focused X-ray beam size was 1.0 \( \times \) 1.0 \( \mu \text{m} \) (full-width at half-max intensity). The sample was scanned in 1-\( \mu \text{m} \) steps [6].

The hydrostatic component of the stress in the Cu TSV was measured in the as-received state as well as during the annealing at 200 \( ^\circ \text{C} \) and finally in the post-annealed state. All the hydrostatic stress measurements were performed on the center of the Cu TSV using monochromatic X-ray beam with 10 keV energy. Cu hydrostatic stress corresponding to the post-annealed state is 167 MPa (tensile), while during the annealing it is –196 MPa (compressive). The hydrostatic stress measurement performed on the same Cu TSV before annealing (i.e. in the as-received state) resulted in a high tensile stress of 234 MPa.

The white-beam (polychromatic) X-ray measurement results were shown in Fig. 2a and b for Cu TSV at the post-annealed condition (after annealing at 200 \( ^\circ \text{C} \) for 1 h). This is presented first as this is the most relevant stress state for practical considerations in terms of reliability and robust integration of a TSV scheme in industry. Fig. 2a shows the grain orientation mapping of the Cu TSV indicating relatively large grains with wide range of orientations. Fig. 2b shows the stress mapping of all the components of deviatoric stresses (normal as well as shear) and their distribution across the TSV domain. The normal deviatoric stresses \( \sigma_{XX}, \sigma_{YY} \) and \( \sigma_{ZZ} \) are basically the full normal stresses \( (\sigma_{XX}, \sigma_{YY} \text{ and } \sigma_{ZZ}) \) without the hydrostatic components (the hydrostatic stresses were measured separately). The shear deviatoric stresses \( \sigma_{XY}, \sigma_{YZ} \) and \( \sigma_{XZ} \) hold their usual meaning. These stress maps suggest the stress state of the Cu TSV is dominated by high shear deviatoric stresses (averaging 145 MPa). The overall stress level corresponding to this post-annealed state is provided by the hydrostatic stress which was already measured to be relatively high tensile of about 167 MPa.

Both the high shear (deviatoric) stresses as well as the relatively high tensile hydrostatic stresses at this post-annealed state could have important implications in terms of reliability and robust integration of the TSV scheme [14,15]. The high tensile hydrostatic stress of 167 MPa here is comparable to the stress level in a conventional Cu interconnect lines [16] and thus could lead to debonding, cracking as well as stress-induced voiding as has been well known in traditional Cu lines, which in turn could lead to degradation of performance of devices and eventually the final catastrophic events of failure of devices. The high shear deviatoric stresses could also lead to plastic damages which could eventually lead to failure of the interconnect device as well.

It is thus important to study the origin of these high stresses and understand how the stresses evolve. Fig. 2c shows the deviatoric stress state of Cu TSV during the high temperature annealing at 200 \( ^\circ \text{C} \) (the measurement was in situ and took 6–7 h to complete). The deviatoric stress state of Cu TSV here shows a much-relaxed state both in terms of the normal as well as the shear stresses compared to the post-annealed state. This is expected as the high

\[ (\sigma_{XX}, \sigma_{YY} \text{ and } \sigma_{ZZ}) \]

\[ \sigma_{XY}, \sigma_{YZ} \text{ and } \sigma_{XZ} \]

\[ (\sigma_{XX}, \sigma_{YY} \text{ and } \sigma_{ZZ}) \]
temperature treatment allows relaxation of stresses both by plastic deformation as well as diffusion. The hydrostatic stress corresponding to this state of during the high temperature annealing was compressive and was about 196 MPa.

These findings thus suggest two things. First, the as-received TSV appears to be already in a very high tensile state of 234 MPa. This could be due to the significant grain growth during room temperature annealing which Cu has been widely known to exhibit [17], that is from the time it was deposited into the TSV structure to the time the stress was measured in this experiment (this period was estimated to be about two months here). Similar room temperature grain growth in Cu TSV has also been previously reported by Okoro et al. [18]. Such grain growth in a confined volume would lead to hydrostatic stress going to the tensile direction due to grain boundary elimination [17].

Furthermore, Fig. 3a shows the cross-section FIB image of a Cu TSV in the as-received state. Cross section of TSV samples were polished by sandpaper and diamond particles and samples were cross-sectioned by Ga ion source with 30 keV in FIB. This FIB image is evident that some of the grains here (especially in the middle of the Cu TSV structure) are larger than grains in the edges of the Cu TSV structure. This indicates there could have been room temperature growth in the middle part of the Cu TSV structure since the time Cu was deposited into the TSV structure (presumably with uniformly fine grain structure similar to those on the edges of the Cu TSV structure) to the time the sample was received by our group for Cu TSV as shown in Fig. 2a and b. This measurement in particular was intended to show the strain/stress profile near the edge of the Cu TSV thus providing insights into the “keep-away” zone information. The measurement error in strain due to uncertainty in instrumental calibration here is $1 \times 10^{-4}$. Both strain profiles ($\varepsilon_{XX}$ and $\varepsilon_{YY}$) show high strains very near to the edge of the Cu TSV (maximum $\varepsilon_{XX} = 6 \times 10^{-4}$ (tensile) and maximum $\varepsilon_{YY} = -4 \times 10^{-4}$ (compressive)). The high strains then reduce to a level which is practically zero ($\pm 1 \times 10^{-4}$) after a distance of about 17 $\mu$m for both $\varepsilon_{XX}$ and $\varepsilon_{YY}$ consistently (shown in Fig. 4b with the black arrows). This thus indicates a “keep-away” zone of about 17 $\mu$m from the edge of the Cu TSV within which the stresses in Si might change the electron mobility of the transistor device significantly such that electrical performance of the device might be out of control.

Stress states of the Cu and Si from our findings indicate that the performance and the reliability of 3-D interconnect could be controlled by the tensile stress of Cu TSV in the as-received state. As such high tensile hydrostatic stress in Cu TSV could be originated from the room temperature grain growth in Cu during the shelf time, one may speculate that any method to minimize the room temperature grain growth in Cu TSV significantly could lead to lower stresses first in the Cu TSV itself and then in turns in the Si surrounding the TSV thus minimizing the reliability concerns as well as the device performance issues.

In summary, the stress state in the Cu TSV is dominated by both high hydrostatic stress as well as high shear stress. Both could lead

---

**Fig. 3.** FIB images showing (a) cross-section of a Cu TSV in the as-received state (approximately two months after the Cu deposition into the TSV structures) and (b) cross-section of another Cu TSV in the post-annealed state (after annealing of 200 °C for 1 h). These images indicate significant grain growth during the annealing phase of 200 °C for 1 h.
to reliability as well as integration issues in the Cu TSV and lead to high stresses in the Si surrounding the Cu TSV which could in turn lead to device performance concerns. Measuring and controlling the stresses and especially how they lead to degradation of the device are thus important in the technology development as well as reliability improvement of the 3-D interconnect schemes.

**Acknowledgments**

The Advanced Light Source is supported by the Director, Office of Science, Office of Basic Energy Sciences, Materials Sciences Division, of the US Department of Energy under Contract No. DE-AC02-05CH11231 at Lawrence Berkeley National Laboratory and University of California, Berkeley, California. The move of the micro-diffraction program from ALS beamline 7.3.3 onto to the ALS superbend source 12.3.2 was enabled through the NSF Grant #0416243. One of the authors (ASB) is supported by the Director, Los Alamos National Laboratory (LANL), under the Director’s Postdoctoral Research Fellowship program (LDRD/X93V). This Project was conducted through the Practical Application Project of Advanced Microsystems Packaging Program of Seoul Technopark, funded by the Ministry of Knowledge Economy, Korea.

**References**


Fig. 4. Si stress state surrounding the Cu TSV showing (a) the measured stress map from the top of the TSV sample as compared to the simulation result performed by other research group [17] and (b) the strain/stress profile from the side of the TSV sample showing the “keep-away” zone from the edge of the Cu TSV of about 17 μm.