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Measurement of stresses in Cu and Si around through-silicon via by synchrotron X-ray microdiffraction for 3-dimensional integrated circuits

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ABSTRACT

Through-silicon via (TSV) has been used for 3-dimentional integrated circuits. Mechanical stresses in Cu and Si around the TSV were measured using synchrotron X-ray microdiffraction. The hydrostatic stress in Cu TSV went from high tensile of 234 MPa in the as-fabricated state, to −196 MPa (compressive) during thermal annealing (*in* situ measurement), to 167 MPa in the post-annealed state. Due to this stress, the keep-away distance in Si was determined to be about 17 μm. Our results suggest that Cu stress may lead to reliability as well as integration issues, while Si stress may lead to device performance concerns.

There is much interest recently in the 3-D interconnects using through-silicon via (TSV) technology in the microelectronics industry due to their potentials for vast improvements in the performance of microelectronics devices as well as their promises in enabling advanced multi-level chips integrating diverse CMOS technologies with each other as well as with emerging technologies such as MEMS and bio-chips [1,2]. One of the key enablers for the successful implementation of 3-D interconnects using TSV is the control of the mechanical stresses in the Cu TSV itself as well as in the surrounding silicon substrate [3,4]. Stresses induced intrinsically by thermal treatment in the TSV interconnect schemes, as well as stresses induced extrinsically, for example due to silicon wafer thinning or chip-package interactions, introduce new reliability challenges for through-silicon via (TSV) technology, while stresses in the silicon substrate surrounding the copper-filled TSV can affect electron mobility in the transistors and thus determine the keep-away zone for Front-End Of Line (FEOL)/chip design [5].

In an effort to shed lights on these topics, the synchrotron-based X-ray microdiffraction technique [6] is the most suitable to measure crystal orientations and stresses in Cu TSV samples. As the high-brilliance synchrotron-sourced X-rays can penetrate and easily distinguish signals of the metallic structures from that of other materials in their surroundings, strain measurements can be done in our samples while the copper-filled TSV is still buried inside the silicon substrate. This allows strain measurements that are as close as possible to conditions in the real operations of the device. Furthermore, this unique capability of the technique also enables us to monitor strains *in situ* during the course of the service of the device.

Past efforts to measure stresses in the 3-D interconnect schemes using TSV technology involved mainly micro-Raman technique [7,8] to measure stresses in the silicon substrate surrounding the Cu TSV and laboratory X-ray diffraction (XRD) technique [8] to obtain average stresses in an array of Cu TSV's. With the synchrotron-based X-ray microdiffraction technique, both stresses in Cu TSV as well as in the Si surrounding it can be measured simultaneously and can thus be compared and their correlation can further be investigated. It is thus another unique advantage of utilizing this technique.

The synchrotron technique of scanning X-ray microdiffraction has been described thoroughly elsewhere [6]. The power of this technique as a local stress probe for micro- and nanoscale devices stems from its two most important features. First, the submicron-sized focused X-ray beam that enables measurement of stresses at submicron resolution. Secondly, the continuous range of wavelengths in the white X-ray beam allows measurements of the deviatoric components of the stresses in addition to the standard ability of an X-ray diffraction technique to measure hydrostatic components of the stress tensors. This technique has proven to be useful in the study of mechanical stresses in advanced microdevices [9] as well as novel micro- and nanoscale structures [10,11]. Impacts of such findings on reliability and robust integration of the devices were also reported [12,13].

The TSV test structure used in this study was electrodeposited at room temperature after metallization and further annealing

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was conducted after TSV fabrication in the present study as specified further in the manuscript. The TSV test structures are of 20 μm diameter and 90 μm height and assembled in an array with 90 μm pitch as shown in Fig. 1.

The synchrotron X-ray microdiffraction experiment was conducted at the Beamline 12.3.2 at the Advanced Light Source (ALS), Lawrence Berkeley National Laboratory (LBNL). Both monochromatic (at 10 keV energy) as well as polychromatic (white-beam, energy scanning was conducted from 9.8 keV to 10.20 keV with 0.01 keV steps) X-rays were used to enable measurements of hydrostatic and deviatoric components, respectively, of the stress tensor. The deviatoric components of the stress tensor in the Cu TSV were studied at the post-annealed state (after annealing at 200 °C for 1 h) as well as during annealing at 200 °C using two different samples. The sample was mounted on a precision XY MICOS stage and the TSV of interest was raster scanned under the focused X-ray beam. The focused X-ray beam size was 1.0 × 1.0 μm (full-width at half-max intensity). The sample was scanned in 1-μm steps [6].

The hydrostatic component of the stress in the Cu TSV was measured in the as-received state as well as during the annealing at 200 °C and finally in the post-annealed state. All the hydrostatic stress measurements were performed on the center of the Cu TSV using monochromatic X-ray beam with 10 keV energy. Cu hydrostatic stress corresponding to the post-annealed state is 167 MPa (tensile), while during the annealing it is −196 MPa (compressive). The hydrostatic stress measurement performed on the same Cu TSV before annealing (i.e. in the as-received state) resulted in a high tensile stress of 234 MPa.

The white-beam (polychromatic) X-ray measurement results were shown in Fig. 2a and b for Cu TSV at the post-annealed condition (after annealing at 200 °C for 1 h). This is presented first as this is the most relevant stress state for practical considerations in terms of reliability and robust integration of a TSV scheme in industry. Fig. 2a shows the grain orientation mapping of the Cu TSV indicating relatively large grains with wide range of orientations. Fig. 2b shows the stress mapping of all the components of deviatoric stresses (normal as well as shear) and their distribution across the TSV domain. The normal deviatoric stresses σ'_{XX}, σ'_{YY} and σ'_{ZZ} are basically the full normal stresses (σ_{XX}, σ_{YY} and σ_{ZZ}) without the hydrostatic components (the hydrostatic stresses were measured separately). The shear deviatoric stresses σ_{XY}, σ_{YZ} and σ_{YZ} hold their usual meaning. These stress maps suggest the stress state of the Cu TSV is dominated by high shear deviatoric stresses (averaging 145 MPa). The overall stress level corresponding to this post-annealed state is provided by the hydrostatic stress which was already measured to be relatively high tensile of about 167 MPa.

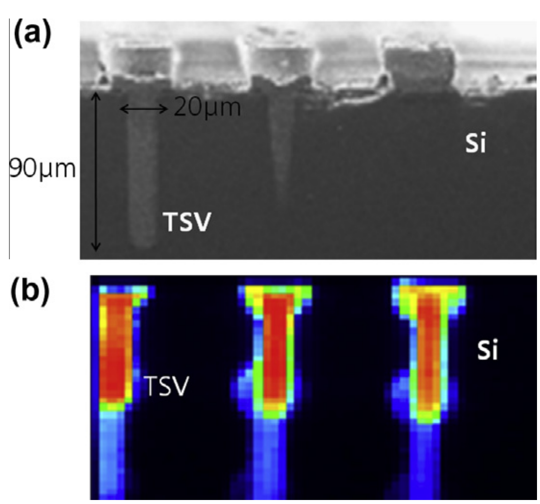

Fig. 1. The TSV test structure: (a) the SEM image that shows the cross-sectioning (by polishing) of an array of TSV's at an angle so that some of the TSV's will be optically visible as shown in the figure and some will still be buried under the silicon substrate thus allowing stress measurements in Cu TSV to be as close as possible to the conditions in the real operations of the device and (b) the synchrotron X-ray microfluorescence (XRF) mapping that shows all the TSV's and thus enable stress measurements and crystal orientation mapping by X-ray microdiffraction (XRD).

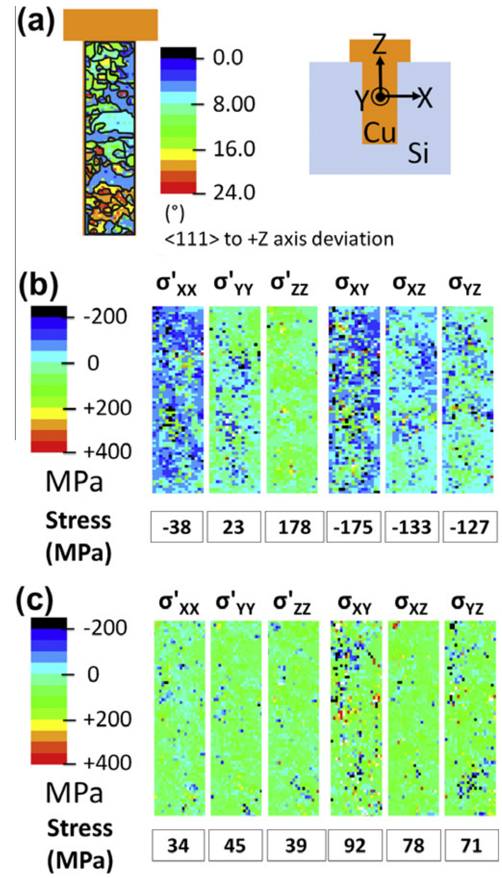

Fig. 2. White-beam X-ray measurement results showing (a) the grain orientation mapping as well as (b) the deviatoric stress mapping of the Cu TSV sample in the post-annealed state (after annealing at 200 °C for 1 h) and (c) the deviatoric stress mapping during the annealing at 200 °C. The XYZ coordinates used here are as described in (a) with respect to the laboratory coordinates. All the stress values on the figure are the average stress of all the stresses from each pixel (1um step size in *X* and *Y* directions) in the measured area of TSV.

Both the high shear (deviatoric) stresses as well as the relatively high tensile hydrostatic stresses at this post-annealed state could have important implications in terms of reliability and robust integration of the TSV scheme [14,15]. The high tensile hydrostatic stress of 167 MPa here is comparable to the stress level in a conventional Cu interconnect lines [16] and thus could lead to debonding, cracking as well as stress-induced voiding as has been well known in traditional Cu lines, which in turn could lead to degradation of performance of devices and eventually the final catastrophic events of failure of devices. The high shear deviatoric stresses could also lead to plastic damages which could eventually lead to failure of the interconnect device as well.

It is thus important to study the origin of these high stresses and understand how the stresses evolve. Fig. 2c shows the deviatoric stress state of Cu TSV during the high temperature annealing at 200 °C (the measurement was *in situ* and took 6–7 h to complete). The deviatoric stress state of Cu TSV here shows a much-relaxed state both in terms of the normal as well as the shear stresses compared to the post-annealed state. This is expected as the high temperature treatment allows relaxation of stresses both by plastic deformation as well as diffusion. The hydrostatic stress corresponding to this state of during the high temperature annealing was compressive and was about 196 MPa.

These findings thus suggest two things. First, the as-received TSV appears to be already in a very high tensile state of 234 MPa. This could be due to the significant grain growth during room temperature annealing which Cu has been widely known to exhibit [17], that is from the time it was deposited into the TSV structure to the time the stress was measured in this experiment (this period was estimated to be about two months here). Similar room temperature grain growth in Cu TSV has also been previously reported by Okoro et al. [18]. Such grain growth in a confined volume would lead to hydrostatic stress going to the tensile direction due to grain boundary elimination [17].

Furthermore, Fig. 3a shows the cross-section FIB image of a Cu TSV in the as-received state. Cross section of TSV samples were polished by sandpaper and diamond particles and samples were cross-sectioned by Ga ion source with 30 keV in FIB. This FIB image is evident that some of the grains here (especially in the middle of the Cu TSV structure) are larger than grains in the edges of the Cu TSV structure. This indicates there could have been room temperature growth in the middle part of the Cu TSV structure since the time Cu was deposited into the TSV structure (presumably with uniformly fine grain structure similar to those on the edges of the Cu TSV structure) to the time the sample was received by our group and cross-sectioning was performed. This is consistent with our above hypothesis.

Secondly, the hydrostatic stress state of Cu seems to largely follow the expansion mismatch with the Si substrate during the heating as well as the cooling of the annealing phase. The $\Delta\alpha\Delta T$ for Cu and Si elements and for the temperature difference associated with the thermal annealing at 200 °C correspond to a stress difference of about 294 MPa which is reasonably close to the actual measured relaxation/increase of hydrostatic stresses in Cu TSV during heating/cooling respectively (430 MPa relaxation and 363 MPa increase). The slight discrepancies could be due to the combination between further grain growth during annealing which has indeed been observed in this experiment as shown in Fig. 3a and b which would strain the crystal further to the tensile direction and plastic deformation during high-temperature annealing that would relax the crystal.

The measurement of stresses in Si surrounding the TSV was done from the top of the TSV rather than from the side as was done for Cu TSV as shown in Fig. 2a and b. The measurement was done only in the post-annealed state with the TSV cap which consists of Cu as well as tin solder materials first removed (by polishing) leaving behind only the Cu TSV with the Si surrounding for the polychromatic X-ray beam scanning. The result was shown in Fig. 4a comparing side-by-side the present experimental findings and the simulation results reported earlier in Ref. [19]. The simulation [19] was based on an analytical solution called Lame solution [20] for a tube with the outer diameter taken here to be infinite and with an inner pressure (or in this case a hydrostatic stress).

The measured stress (σ_{XX}) map here bears a rather close resemblance to the simulation result based on the Lame solution/model [19,20]. The measured σ_{XX} on the right and left hand sides of the TSV is mostly tensile whereas on the above and below of the TSV it is mostly compressive – a trend that is largely and qualitatively consistent with the simulation result [19,21,22]. This close resemblance to the Lame solution/model strongly indicates that the stress state in the Si surrounding the TSV is largely controlled by the hydrostatic component of the Cu stress state (i.e. the "inner pressure" of the "tube" in the Lame solution) in the TSV.

Fig. 4b shows the measurement of the ε_{XX} and ε_{YY} which was done from the side – similar to the Cu TSV stress measurement in Fig. 2a and b. This measurement in particular was intended to show the strain/stress profile near the edge of the Cu TSV thus providing insights into the "keep-away" zone information. The measurement error in strain due to uncertainty in instrumental calibration here is 1×10^{-4}. Both strain profiles (ε_{XX} and ε_{YY}) show high strains very near to the edge of the Cu TSV (maximum $\varepsilon_{XX} = 6 \times 10^{-4}$ (tensile) and maximum $\varepsilon_{YY} = -4 \times 10^{-4}$ (compressive). The high strains then reduce to a level which is practically zero ($\pm 1 \times 10^{-4}$) after a distance of about 17 μm for both ε_{XX} and ε_{YY} consistently (shown in Fig. 4b with the black arrows). This thus indicates a "keep-away" zone of about 17 μm from the edge of the Cu TSV within which the stresses in Si might change the electron mobility of the transistor device significantly such that electrical performance of the device might be out of control.

Stress states of the Cu and Si from our findings indicate that the performance and the reliability of 3-D interconnect could be controlled by the tensile stress of Cu TSV in the as-received state. As such high tensile hydrostatic stress in Cu TSV could be originated from the room temperature grain growth in Cu during the shelf time, one may speculate that any method to minimize the room temperature grain growth in Cu TSV significantly could lead to lower stresses first in the Cu TSV itself and then in turns in the Si surrounding the TSV thus minimizing the reliability concerns as well as the device performance issues.

In summary, the stress state in the Cu TSV is dominated by both high hydrostatic stress as well as high shear stress. Both could lead

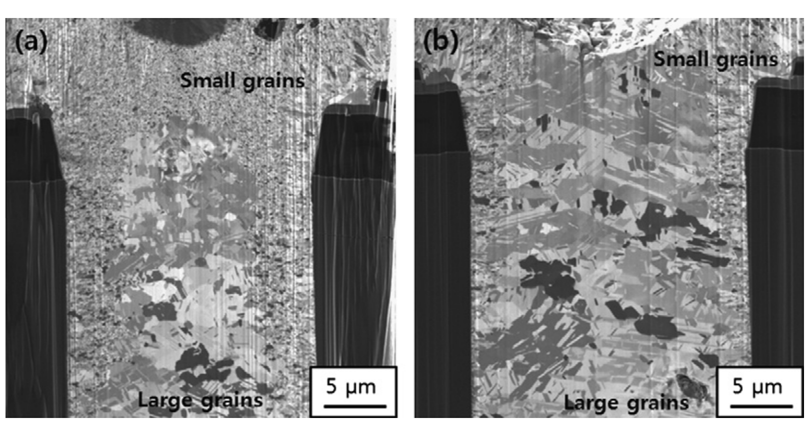

Fig. 3. FIB images showing (a) cross-section of a Cu TSV in the as-received state (approximately two months after the Cu deposition into the TSV structures) and (b) cross-section of another Cu TSV in the post-annealed state (after annealing of 200 °C for 1 h). These images indicate significant grain growth during the annealing phase of 200 °C for 1 h.

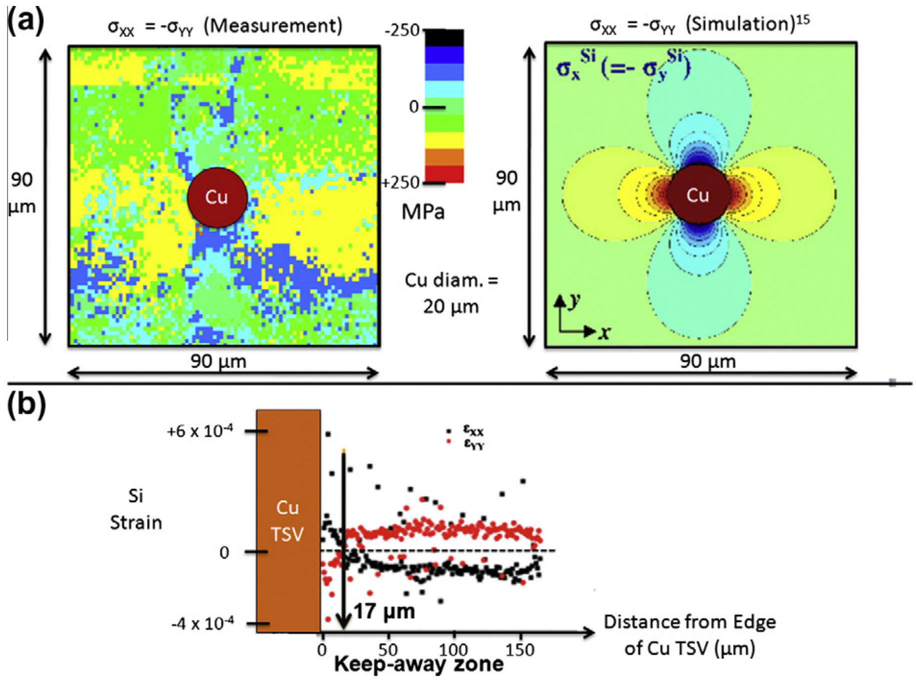

Fig. 4. Si stress state surrounding the Cu TSV showing (a) the measured stress map from the top of the TSV sample as compared to the simulation result performed by other research group [17] and (b) the strain/stress profile from the side of the TSV sample showing the "keep-away" zone from the edge of the Cu TSV of about 17 µm.

to reliability as well as integration issues in the Cu TSV and lead to high stresses in the Si surrounding the Cu TSV which could in turn lead to device performance concerns. Measuring and controlling the stresses and especially how they lead to degradation of the device are thus important in the technology development as well as reliability improvement of the 3-D interconnect schemes.

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