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Critical temperature shift for Stress Induced Voiding in Advanced Cu Interconnects for 32 nm and beyond.

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Abstract

Work showing evidence of a shift in the Stress Migration (SM) peak profile temperature for smaller interconnect linewidths typically associated with the 32 nm technology node and beyond is presented here. With other parameters (fabrication, materials, line thickness and via diameter being kept nominal among all these samples), this clear shift towards the lower temperatures for smaller linewidths appear to indicate a size effect in the Stress Migration in advanced Cu interconnect scheme. The synchrotron x-ray micro-diffraction experiment, is used to show that plasticity is involved in the stress relaxation process at about 200° C, but not at higher temperature nor at room temperature. Such plasticity-assisted strain relaxation in interconnects especially at lower temperature range could explain the critical temperature shift observed in the present study, in addition to the typical diffusion-assisted mechanism. Further, the synchrotron X-ray micro-diffraction experiments also suggests indications of plasticity-assisted voiding. Numerical finite element analyses were also conducted in conjunction with the experimental study, to provide greater insight. The modelling result demonstrates the importance of creep plasticity in causing thermal stress relaxation in Cu interconnects.

Keywords: Copper; Interconnects; Stress Induced Voiding; Stress Migration; Reliability; Plastic Deformation; Modeling; FEM;

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1. INTRODUCTION

A key challenge for advanced Integrated Circuit (IC) generations (32nm and beyond) is the Stress Induced Voiding (SIV) or Stress Migration (SM) in interconnects [1-2]. The margin for reliability of copper based interconnect systems is ever shrinking. Manufacturing is impacted by material selection, design rules and test structure design. The key for designing robust components for advanced technology nodes is indeed in the understanding of the factors that trigger the onset of SIV.

2. EXPERIMENTAL

In this study the typical SM daisy chain structures (M1/M2) which is a variation of a BEOL process for a 32nm CMOS technology fabricated by Vitesse Semiconductor Corp was used as the interconnect test structure. Samples of 4 different line-widths were used (4.5, 2.0, 0.9, 0.4 µm) with all having the same via diameter, overlay as well line length and thickness. Typical SM reliability testing (thermal loading) were conducted at six different temperatures (110, 135, 170, 195, 225 and 255° C) with electrical resistance measurements. The resistance increase after about 400 hours of SM baking based on 10 DUT's (Device Under Testing) for each test temperature for each linewidth is shown in the Fig. 1. To study plasticity and mechanical stresses in the device and to understand how the stress evolution during the device's real and accelerated service conditions in situ synchrotron-based white-beam (Laue) X-ray micro-diffraction technique (ALS, Berkeley Lab) was used. The synchrotron technique of scanning white beam X-ray micro-diffraction has been described in a complete manner in a previous publication [3].

The synchrotron-based X-ray micro-diffraction technique [3-6] is a non-destructive micron resolution method to measure crystal orientations and stresses in the samples. As the high-brilliance synchrotron-sourced X-rays can penetrate and easily distinguish signals of the metallic structures from that of other materials in their surroundings, strain measurements can be done in the samples easily [7]. This allows strain measurements that are as close as possible to conditions in the real operations of the device. The focused X-ray beam allows stress measurements in the submicron regime. Further, the white x-ray beam provides a white range of wavelengths that allows deviatoric stress component measurements in addition to the traditional x-ray diffraction technique to measure hydrostatic components of the stress tensors. This synchrotron-based X-ray micro-diffraction technique has also been used to investigate microstructure-controlled or stress-controlled reliability as well as performance issues in advanced microelectronics [8-11], nanotechnologies [12-17] along with next generation energy systems [18-22].

3. RESULTS AND DISCUSSION

Stress migration temperature profile has been widely recognized and first reported by McPherson and Dunn [23].

$$\frac{\Delta R}{R_o} = C(T_o - T)^N \exp\left(\frac{E_A}{KT}\right) \qquad (1)$$

The McPherson-Dunn equation above (Eq. 1) describes how SM resistance increase (ΔR and R_o are resistance increase and initial resistance respectively) depends on two factors: the tensile stress in the metal as the driving force of voiding and the diffusion (C, T_o, T, N, E_A and K are empirical coefficient, stress-free temperature, test temperature, creep exponent, activation energy for vacancy diffusion, and universal gas constant, respectively). The stress component decreases as temperature approaches stress-free temperature (which is typically about 300-400 °C for Cu thin films for example) while the diffusion component always increases as temperature increases thus the profile with a peak in the intermediate temperature. Voiding is minimum at low temperatures because even though stress is high, diffusion is low, meanwhile voiding is also minimum at high temperatures because even though diffusion is high, stress which is the driving force for voiding is low. At some intermediate temperatures, voiding is worst because both driving force and diffusion are enabled.

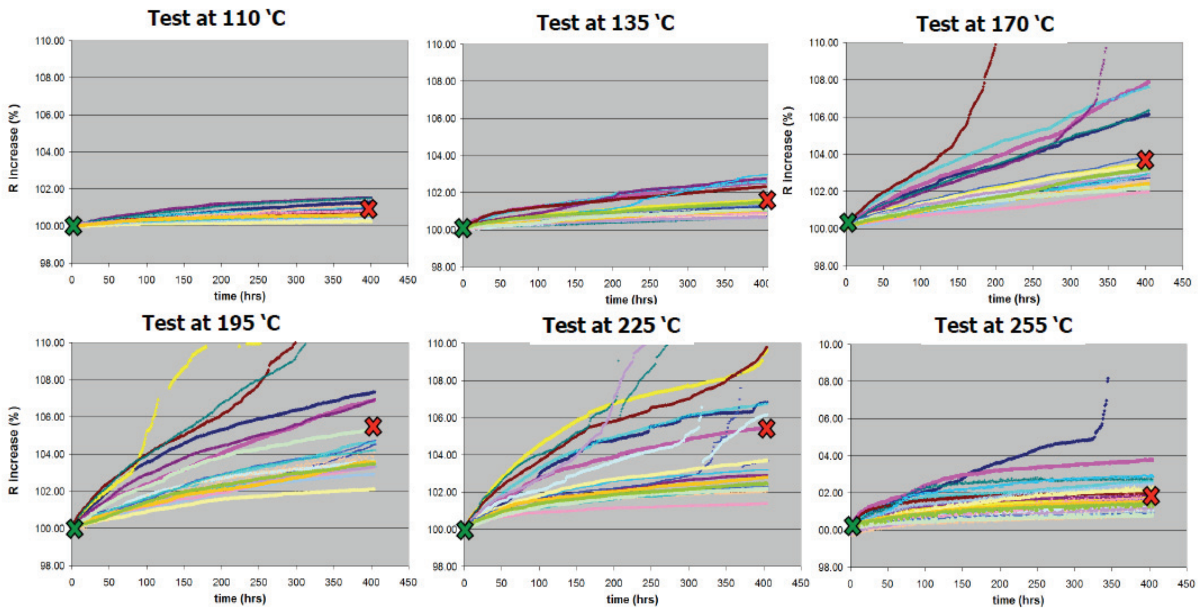


Fig. 1. Typical SM Test Measurements: ΔR/R vs. Time

There appears in the present study to be a clear shift in the SM peak towards lower temperature as we go towards smaller and smaller line-widths (representing the more advanced technology nodes) as shown in Fig. 1. The experimental data of resistance increase as a function of test temperature for each linewidth could be fit into the McPherson-Dunn equation above and from that fitting all the unknown parameters (***C***, $\boldsymbol{T_0}$, ***N*** and $\boldsymbol{E_A}$) could be determined. Table 1 provides all the parameters for each of the sample linewidths with the best fitting

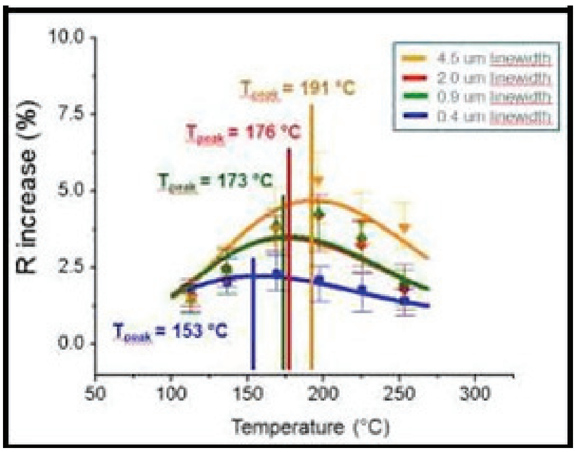


Fig. 2. Stress Migration temperature profiles for Cu samples with different linewidths. The data point represents the median value while the error bar represents the range of all data (10 DUT's per test temperature per linewidth).

	0.4 μm linewidth	0.9 μm linewidth	2.0 μm linewidth	4.5 μm linewidth
T_0 (°C)	350	350	350	350
E_a (eV)	0.71	0.77	0.78	0.79
N	5.89	3.96	4.11	2.84
C	8.75E-08	5.92E-07	6.06E-07	6.78E-09
R^2 stdev	0.04	0.11	0.08	0.09
T_{peak} (°C)	153	173	176	191

Table 1. McPherson-Dunn parameters experimentally obtained by fitting the electrical resistance data for each linewidth samples.

As the SM peak temperature shifts to the lower temperatures for the smaller linewidths, it is apparent from Table 1 that while $\boldsymbol{E_A}$ is relatively constant (from the best fitting), the creep exponent, ***N***, increases as linewidth gets smaller and smaller (representing the advanced technology nodes). The largest linewidth of 4.5 µm has ***N*** equals to 2.84 which is a typical value for bulk ductile metals, whereas the narrowest linewidth of 0.4 µm has ***N*** equals to 5.89 which from metals creep references usually represents work-hardened metals. Higher creep exponent, ***N***, usually means there are more mechanisms for the metal to creep, such as dislocation motion, dislocation multiplication, etc. Insertion of any kind of obstruction to dislocation motions usually leads to higher ***N*** value [24]. This trend of increasing ***N*** with narrowing linewidth may be significant and could potentially lead to the explanation of why the SM peak temperature shifts to lower temperatures.

As fabrication process is nominal, this shift towards lower temperature could thus be a size effect in which dislocation motion and processes may play a more important role as compared to in the more typical Stress Migration events. It appears that while SM voiding in the larger linewidths are mostly governed by the stress driving force and diffusion as in the McPherson-Dunn equation, the SM voiding in the narrow linewidths could be controlled in addition by plasticity (dislocation motion, multiplication, etc.). This could make sense as in the lower temperatures (such as 153 °C for the 0.4 µm linewidth samples) diffusion is likely to play smaller role, whereas plasticity could still be activated as it is mostly driven by the high stress in the metals. More importantly, the stress state of narrow lines is more likely to be triaxial rather than biaxial in the wider lines (i.e. closer to stress state of thin films) thus providing higher shear stresses which are driving force for dislocation motion and activities. This lower temperature mode is more dangerous as it is closer to real operational condition of microelectronics devices. This is especially a going concern for the upcoming advanced technology nodes (32 nm and beyond) with smaller and smaller linewidths and via dimensions.

A. Synchrotron X-ray Micro-diffraction

We have some preliminary evidence that plasticity could play a more prominent role in the lower temperature range. Our synchrotron results show plasticity in advanced Cu interconnect lines undergoing thermal stressing, not at the highest of stress temperatures, but instead at a rather low temperature of 200 °C.

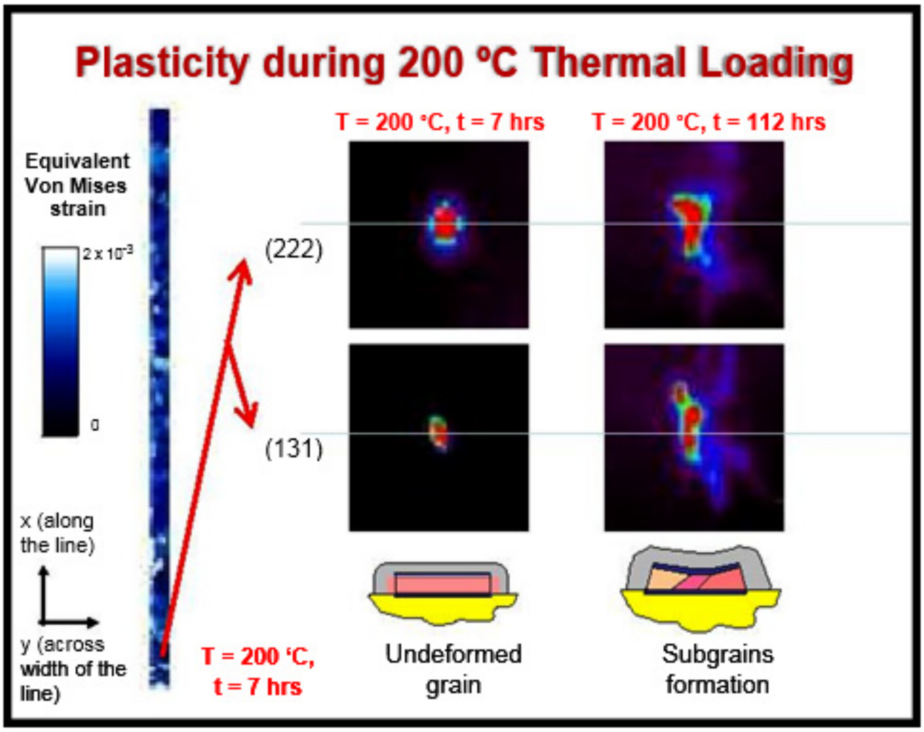
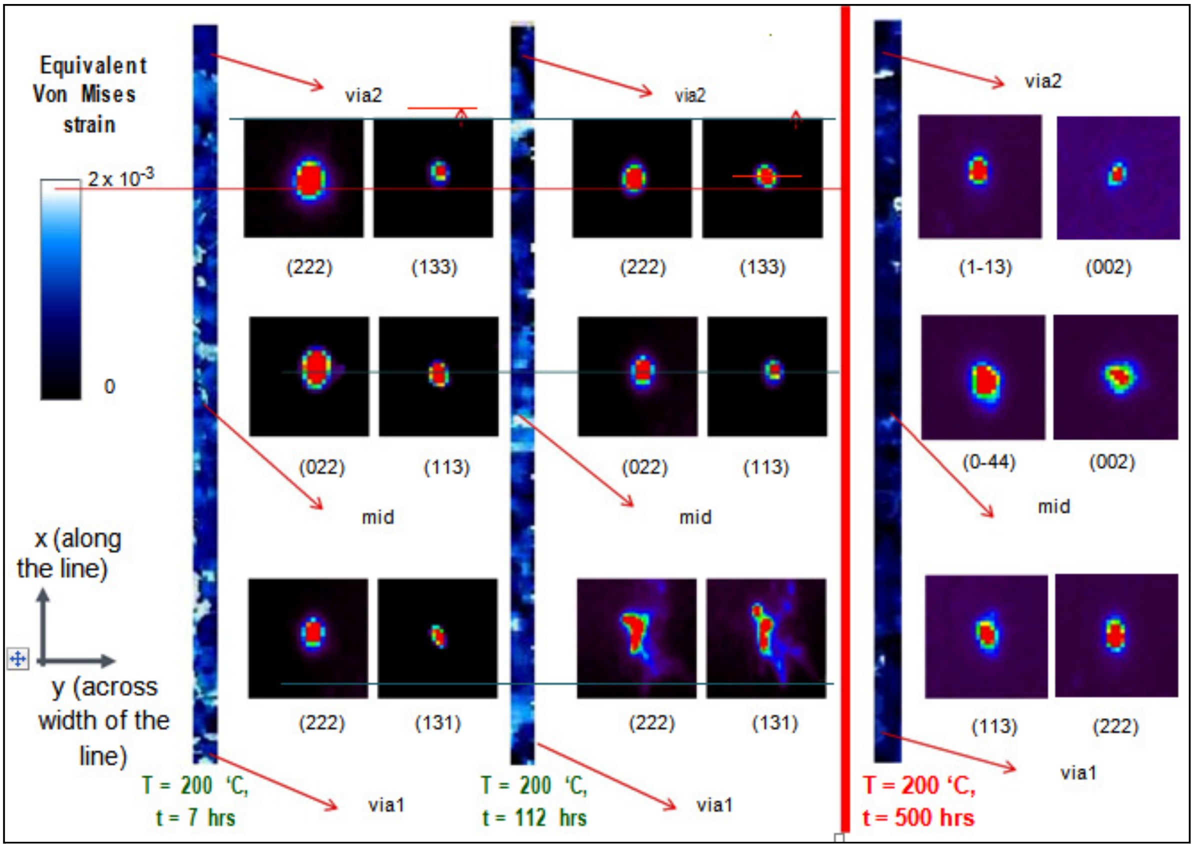


Fig. 3. Plasticity during 200°C thermal loading in 2 μm-wide interconnect line. Streaked (asymmetrically broadened) Cu Laue peaks were observed in one end of the M2 line segment (length = 20 μm) just above the via as shown above (red arrow) after about 100 hrs of thermal loading. Similar observation was found with the 4.5 μm-wide sample.

The plasticity here manifests in the form of asymmetric broadening of Cu Laue peaks observed in both the 2 μm- (Fig. 2) and 4.5 μm-wide interconnect lines. In situ Laue synchrotron X-ray micro-diffraction study could not be performed here for lines with 0.9 μm and 0.4 μm linewidths due to lack of resolution (Focused X-ray beam size is about 0.8 μm x 0.8 μm). Only one segment of M2 lines each from the 2 μm and the 4.5 μm-wide samples were scanned due to limited experimental time in the ALS Beamline 12.3.2. Plasticity in the advanced Cu interconnect and its observation using the synchrotron X-ray micro-diffraction technique has been reported earlier [4].

Similar interconnect samples undergoing thermal stressing at a higher temperature of 350 °C did not exhibit such asymmetric broadening of Cu Laue peaks in the post-mortem study conducted by synchrotron Laue X-ray micro-diffraction, indicating that no significant plasticity was involved during the thermal treatment. At such high temperature, stress in the metal lines could be mostly relaxed through voiding by vacancy diffusion. The samples in the present study however did not show observable voiding. This could be due to limited thermal stressing/baking time in the beamline experiment (only ~ 100 hours). These observations thus suggest that plasticity was involved in the thermal stress relaxation during low temperature loading (in addition to vacancy diffusion). We also have evidence (Fig. 4) that the strain mapping of the interconnect line after some period of thermal loading does show a general stress level that is substantially lower than that of the beginning of the thermal loading. This plastic relaxation during thermal loading is again only at low-intermediate temperatures (not high temperatures, not room temperature). Fig. 4 shows basically an evolution of the same interconnect line through a thermal loading/baking experiment (for 500 hours) as observed by synchrotron X-ray micro-diffraction with Laue (white-beam) technique.

Each of the figures (a), (b) and (c) shows the von Mises strain map of the interconnect line and some samples of Cu Laue reflection peaks that were observed during the baking from three different locations in the line (via 1, via 2 and the mid of the line). The evolution of what happens inside the interconnect line was recorded at (a) at time equals to 7 hours, at (b) at time equals to 112 hours and finally at (c) at time equals to 500 hours of the thermal loading/backing experiment. The first thing to note is the evidence of plasticity at via 1 as has been discussed in Fig. 3 and in the paragraphs above. However in Fig. 4(b), it also became clear how the plasticity led directly into the strain release right in the area where we took the Laue portraits from (i.e. in via 1). This is evident from the strain mapping. As we can see, the strain mapping of Fig. 4(b) shows much darker color in via 1 area, which indicates much lower von Mises stress. This is a strong indication that the metal stress has been relaxed by plasticity, in addition to by vacancy diffusion, especially at low-intermediate temperatures. It is also evident that other areas in the interconnect line not showing evidence of plasticity (i.e. asymmetric broadening of Laue peak shape) did not show much strain relaxation.



(a) **(b)** **(c)**

Fig. 4. . Complete evolution of a Cu interconnect line (2um width, 20um length), which is the same interconnect line in Figure 3, in terms of von Mises strains and Cu Laue reflection peak shapes during a 500-hrs thermal loading/baking experiment; (a) at time equals to 7 hrs, (b) at time equals to 112 hrs and finally (c) at time equals to 500 hrs of the thermal loading/backing experiment.

Yet, further and perhaps more interestingly, Fig.4(c) shows two things: first, the strain map of the line is now in general much darker indicating the whole line has become much more relaxed, and secondly there is yet another significant change with the Laue peaks from via 1 area. Let's discuss the latter first. It is evident that the Laue peaks that were asymmetrically broadened in Fig.4 (b) now have become rounded again in shape, indicating the absence of excess geometrically necessary dislocations (GND's). While we don't have yet the microstructural evidence, we believe the Laue peak shape evolution as shown in Figs. 4(b) and (c) indicates plasticity-assisted voiding. Or in other words, a crystal with many excess GND's could only rid itself of those excess dislocations by creating voids and then storing the excess dislocations in the voided volumes. This observation is thus another indication of how voiding could be both assisted by vacancy diffusion as well as by plasticity, especially at lower and intermediate temperatures. Indeed, this could be the explanation of the shift to the lower temperature as we observed in Fig. 2 in this present study. This is also the reason that Fig. 4(c) also shows in general the strain map of the whole line becomes much darker indicating much less stress. This could be the combination of voiding due to diffusion and plasticity. Perhaps just in general after 500 hours of baking, significant vacancy diffusion has occurred, and more and more voids are created. Due to the availability of these voided volumes, it becomes easier for crystals with many excess dislocations to rid themselves of the excess dislocations and thus creates maximum strain release.

B. Numerical Modeling

Three-dimensional finite element modeling was carried out to examine the thermal stress relaxation behavior of Cu during the constant-temperature hold time at different temperatures. The model includes two levels of Cu lines connected by a via, with the metal structure embedded within the SiOx dielectric. All nitride barrier and etch stop layers are also included. The Cu material is taken to be elastic-plastic with strain hardening [25]; its time-dependent response is provided by a creep plasticity constitutive model based on the power-law creep [26]. All other materials are assumed to be elastic. The simulations include a first cooling step from the initial stress-free temperature (taken to be 350 ºC), and a heating step to the targeted "test temperature" (or staying at 20 ºC). One hundred hours of constant-temperature dwell then ensues. The primary objective is to examine the evolution of stress relaxation and deformation at the different temperatures, to offer insight into the x-ray micro-diffraction experimental result.

The time-dependent FEM model shows significant stress relaxation through plastic deformation (creep) during thermal loading at the intermediate temperature of 200 °C. Stress relaxation also occurred during thermal loading at 350 °C but the initial stress values were low to begin with, therefore no significant creep was observed. The case of 20 ºC loading did feature high magnitudes of thermal stress in Cu, but the temperature is too low for creep plasticity to take effect. Fig. 5. Shows the equivalent creep strains in Cu at the end of 100 h at (a) 20, (b) 200 and (c) 350 ºC. By comparing the strain magnitudes it is evident that the case of 200 ºC shows the most significant creep**.**

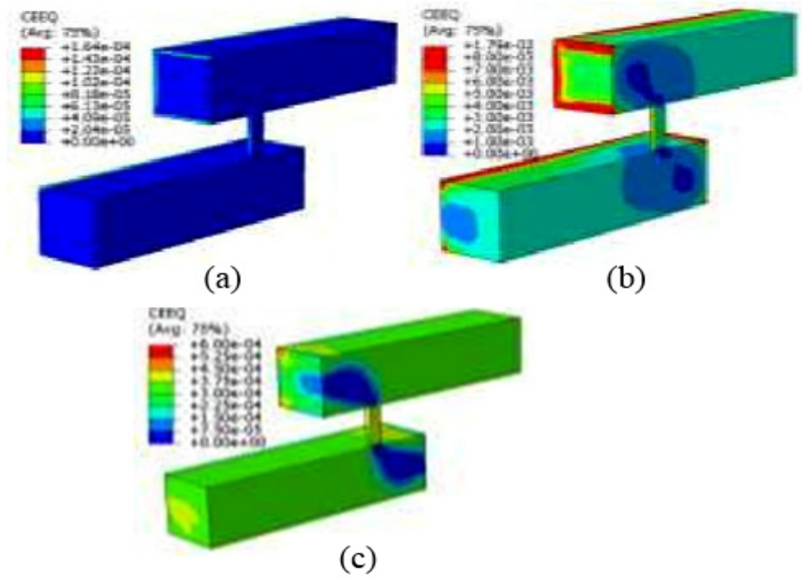


Fig. 5. Simulated equivalent creep strain in the Cu lines and via after 100 h at (a) 20 ºC, (b) 200 ºC and (c) 350 ºC.

4. CONCLUSION

Some preliminary evidences of a plasticity-assisted strain relaxation model were obtained from our experimental and modelling work. This can explain why SM worst case temperature is lower for smaller interconnect lines. A clear shift in the SM peak shift towards lower temperatures is observed as we go towards smaller line-widths (representing the more advanced technology nodes of 32nm and beyond). This could have both technological and industrial importance as we move to even smaller technology nodes. The SM worse temperatures could then approach normal operating temperatures of devices and thus the reliability of the devices would become an important issue.

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