Effect of Interconnect Plasticity on Soldering Induced Residual Stress in Thin Crystalline Silicon Solar Cells

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Abstract

Soldering of copper interconnects at ~220 °C induces residual stresses in the crystalline silicon solar cells. These residual stresses may become detrimental in the context of thinner silicon cells (<180μm) causing cracking, performance loss and failures. In such a scenario a systematic evaluation of these residual stresses considering realistic material properties is required to assess the risk levels. In the present work, soldering induced residual stresses in the back contact c-Si solar cells were evaluated using finite element simulations. Effect of plasticity of the copper interconnects on the cell residual stress was studied. It was observed that the linear elastic material property of interconnect and solder over predicts the cell stress significantly and hence elastic-plastic material properties are needed for realistic predictions. Simulated stresses were also compared with those of synchrotron X-ray micro-diffraction experiments for cell thickness of 180μm to validate the finite element model. Further residual stress was evaluated as a function of silicon cell thickness in order to assess the risk of thinning cells for the current soldering process. These results are expected to enable optimization of soldering and interconnect parameters to mitigate high residual stress and thereby cell fractures.

1 Introduction

Despite being the most dominating in the field, the crystalline silicon (c-Si) photovoltaic (PV) technology has widely reported reliability issues due to the brittle nature of crystalline silicon. International Energy Agency (IEA) review on failures of photovoltaic modules revealed that ~10% of the failures are due to cell interconnects [1]. In the PV modules, individual c-Si cells are interconnected using copper ribbons by soldering. Cell soldering process requires high temperatures close to 220 °C, which induces residual stresses in them due to CTE mismatch [2-5]. These residual stresses may lead to micro cracks in the c-Si cells or cause fracture of the cells due to propagation of existing cracks [2-5]. Recent technological improvements to reduce cost are driving thinner silicon wafers, which in turn intensify these thermo-mechanical residual stresses [2-4]. Hence a systematic evaluation of the soldering induced residual stresses is necessary to assess the risk levels and device mitigation plans. Finite element analysis (FEA) is being widely used to simulate mechanical failures of c-Si solar PV modules at a lower cost (compared to experiments) with reasonable accuracy and ease [6-12]. However realistic material properties need to be used in FEA simulations to get meaningful results. In the present work soldering induced residual stress in a back contact (for ex. Sunpower) mono crystalline silicon solar cell was simulated using FEA. Effect of elastic vs. elastic-plastic properties of the copper interconnect and solder material on the residual stress was studied. Further the effect of cell thickness reduction on the residual stress was also evaluated using parametric FEA simulations. The simulation results were also validated against the experimental results obtained from Synchrotron X-ray Micro-diffraction (μSXRD) [13-19] for a nominal cell thickness (180 μm).

2 Finite Element Modeling and Analysis

Fig. 1 shows schematic of a soldered string of back contact mono crystalline silicon solar cells. Each cell was soldered at 3 locations to a typical dog-bone interconnect made of tin coated copper ribbon. The nominal dimensions (in mm) of the components are also shown in Fig. 1.

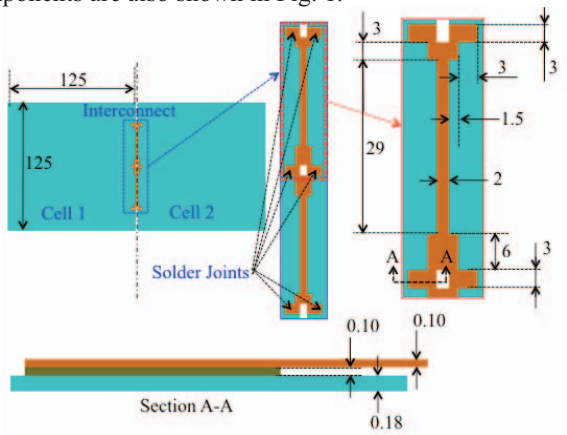

Fig. 1. Schematic of soldered c-Si cells (dimensions in mm, not to scale)

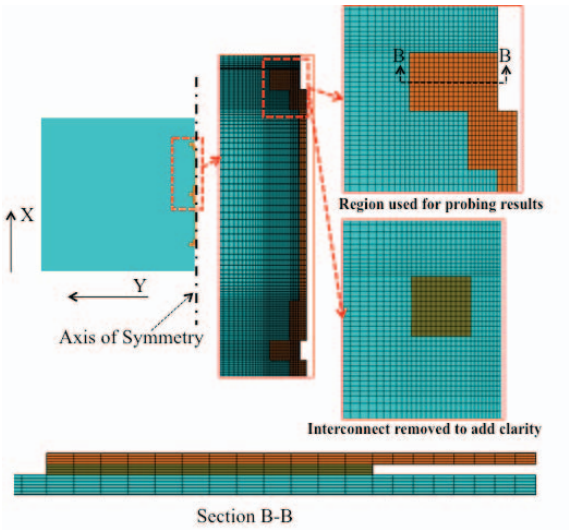

Fig. 2. Finite element model details

An FEA model shown in Fig. 2 was developed based on the dimensions shown in Fig. 1 using commercial FEA code,

ABAQUS [20]. The FEA model assumes symmetry about the central axis along the length of the copper interconnect and hence only 1 cell and half of the interconnect was modeled as shown. In order to make the model computationally inexpensive, intricate geometric details (ref. Fig. 3) of the copper interconnect were omitted and solder joint was idealized to be under the interconnect tab as shown in Fig. 2. Back metallization of the cell (ref. Fig. 3) was not considered due associated modeling difficulties and unavailability of the geometric parameters. Its effect was assumed to be the same in all the cases studied in this manuscript. The model was meshed with 8 node linear quadrilateral elements of area ~0.3 mm^2 around the solder joint and the cell thickness (180 μm) was divided into 6 layers as shown to capture local high stresses in the c-Si cell. Anisotropy of the silicon elasticity was considered as given by Eqn (1) [21] and the elastic material properties of the cell, interconnect and solder, given in Table 1 [9-10, 22] was used in the analysis.

Elasticity tensor of c-Si <100> in GPa,

$$C = \begin{bmatrix} 166 & 64 & 64 & 0 & 0 & 0 \\ 64 & 166 & 64 & 0 & 0 & 0 \\ 64 & 64 & 166 & 0 & 0 & 0 \\ 0 & 0 & 0 & 80 & 0 & 0 \\ 0 & 0 & 0 & 0 & 80 & 0 \\ 0 & 0 & 0 & 0 & 0 & 80 \end{bmatrix} \quad (1)$$

Elastic-plastic behavior of the interconnect and solder was also considered in this analysis and the respective plastic properties were given in Table 2 [10, 23]. The model was constrained at the bottom most node of the cell below the middle solder joint to arrest rigid body motion. The CTE mismatch was simulated by steady state response of the model upon cooling from uniform soldering temperature of 210 °C to room temperature, 25 °C.

Table 1. Elastic Material Properties [9-10, 22]

Material	Young's Modulus, E		Poisson's Ratio	CTE (mm/mm/deg C)	
	Value	Temperature (deg C)		Value (PPM)	Temperature (deg C)
Silicon	Eqn (1)	---	0.28	1.72	-53
				2.23	-13
				2.61	27
				2.92	67
				3.34	147
Copper (Interconnect)	91.5	-40	0.3	17	---
	85.7	25			
	82	125			
	79.2	225			
Solder (Sn-Ag-Cu)	53	0	0.35	21	---
	45	100			
	36	200			

Table 2. Plastic Material Properties [10, 23]

Material	Yield Stress (MPa)	Tangent Modulus (MPa)	Temperature (deg C)
Copper (Interconnect)	116.2	1000	-40
	95.1	1000	25
	82	1000	125
	79.2	1000	225
Solder (Sn-Ag-Cu)	45	-	25
	28	-	180
	25	-	210

3 Experimental

Changes in crystal orientation of the solar cell sample of nominal thickness (~180 μm) as shown in Fig. 3 were measured with μSXRD on beamline 12.3.2 of the Advanced Light Source, Berkeley, CA. The experimental procedure was discussed elsewhere [13-14]. Further details on μSXRD technique, Synchrotrn X-ray beam and data analysis can be obtained from from references [15-19]. From the data analysis of μSXRD scan [18], the mis-orietation angles (φ_x, φ_y) of the c-Si wafer with respect to the undeformed wafer mid plane (XY plane) were obtained. Then curvatures of the wafer (κ_{xx}, κ_{yy}) with respect to X and Y-axes can be calculated using Equations (2) and (3).

$$\kappa_{xx} = -\frac{\partial \varphi_y}{\partial x}\Big|_{y=const}, \ \varphi_y \text{ in radians} \quad (2)$$

$$\kappa_{yy} = \frac{\partial \varphi_x}{\partial y}\Big|_{x=const}, \ \varphi_x \text{ in radians} \quad (3)$$

Using assumptions similar to Kirchhoff plate model [23], the bending strains of the silicon cell can be calculated from curvatures by Equations (4) and (5).

$$\varepsilon_{xx} = -\frac{t}{2}\kappa_{xx}, \text{ '}t\text{' is thickness of the c-Si cell} \quad (4)$$

$$\varepsilon_{yy} = -\frac{t}{2}\kappa_{yy} \quad (5)$$

Since the silicon cell is very thin, assuming the through thickness normal stress (σ_{zz}) to be zero let us calculate the cell bending stresses (σ_{xx}, σ_{yy}) using Hooke's law. The results were presented in the following sections.

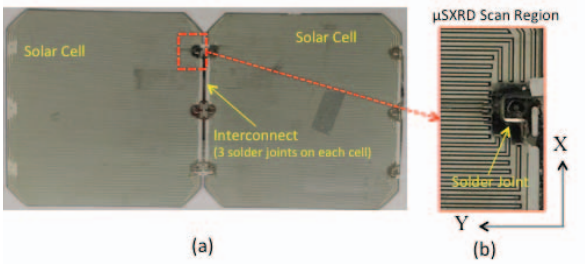

Fig. 3. (a) Experimental sample of the soldered cells, (b) μSXRD scan region

4 Results & Discussion

In this manuscript the primary focus is on the residual stresses induced by soldering process and the solder joints indeed act as the stress concentration zones, so we limit our discussion of results to the solder joint. Stress contours in the 180 μm thick c-Si cell surrounding the solder joint considering both elastic and elastic-plastic material properties are shown in Fig. 4. It can be noted that the stresses are concentrating around the solder joint and high in-plane stresses are seen with elastic material properties which reduced significantly upon using elastic-plastic material properties for copper interconnect and solder. The maximum X-direction stress with elastic properties was 176 MPa, which reduced to 133 MPa upon incorporating copper interconnect plasticity and further reduced to 81 MPa upon incorporating solder material plasticity. The reduction of stress is very significant (>50%) and can't be ignored. Similarly the Y-direction stress reduced from 99 MPa to 69 MPa (>30% reduction). Fig. 5 shows the

experimental stress maps of 180 µm thick back contact mono crystalline silicon cell obtained by µSXRD. The FEA stress contours with elastic plastic material properties (Fig. 4c) compare well with these experimental stress maps, which validates our FEA model. These results also show that the plasticity (or ductility) of the interconnect and solder play crucial role in reducing soldering induced stresses. An alloy material, which is less stiff and more ductile, compared to copper may be a better choice for interconnection to reduce stresses. Or it may be even better to engineer such material.

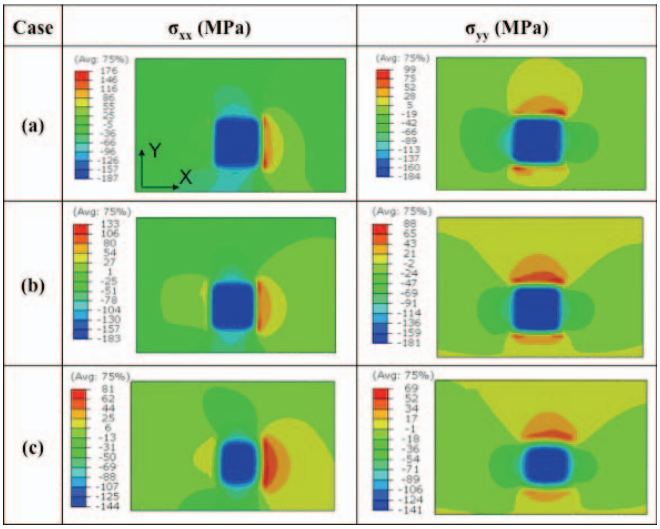

Fig. 4. Post soldering residual stresses of 180 µm thick silicon cell from FEA simulations, (a) with Elastic material properties, (b) with elastic-plastic copper interconnect and elastic solder, (c) with elastic-plastic copper interconnect and solder

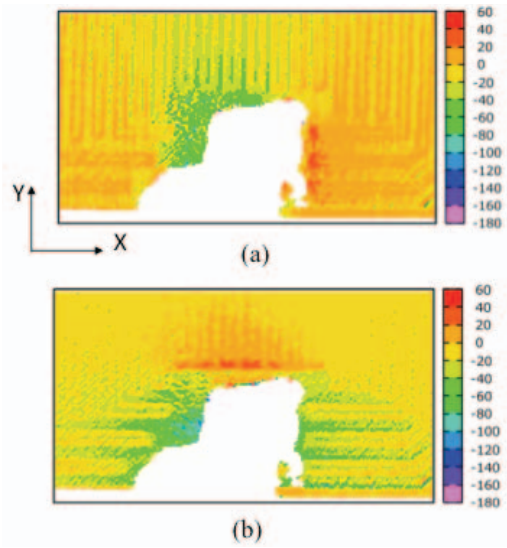

Fig. 5. Post soldering residual stresses of 180 µm thick silicon cell from µSXRD, (a) X-direction stress, (b) Y-direction stress

Further the effect of silicon cell and interconnect thickness on the cell residual stress was simulated (Fig. 6). It can be seen from Fig. 6a that the X-direction stress is increasing almost linearly with reduction in cell thickness and the Y-direction stress is reducing, which in turn increases the in plane max principal stress, hence tendency to fracture. However decreasing the copper interconnects thickness can counterbalance the reduction in cell thickness. It can be seen from Fig. 6b that the stresses reduce due to reduction interconnect thickness. Similarly the thickness of the solder may also affect the residual stresses, which was not studied in this manuscript.

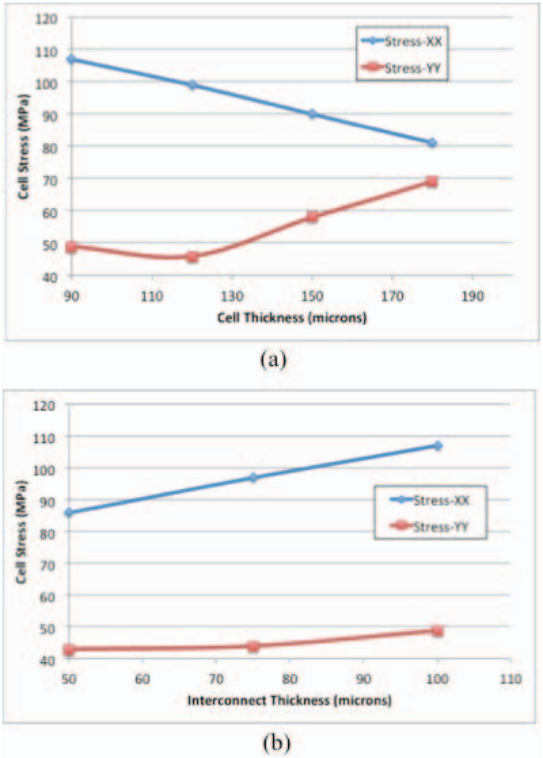

Fig. 6. Post soldering residual stresses of silicon cell from FEA simulations considering elastic-plastic material properties for interconnect and solder, (a) for varying cell thickness, (b) for varying interconnect thickness (cell thickness 90 µm)

Conclusions

The effects of copper interconnect and solder plasticity on the silicon cell residual stresses were simulated using FEA. The residual stress depends significantly on the interconnect plasticity and hence a less stiff and ductile alloy may become a better choice for solar cell interconnection. The FEA results match well with the experimental results. Further the effect of silicon wafer (cell) thickness on the cell residual stress was also evaluated to show that residual stress in the cell increases linearly with cell thickness reduction. Further it was noted from the simulations that the reduction in cell thickness can be counterbalanced by reducing the interconnect thickness to curtail stress levels. These preliminary results are encouraging and inspire us to evaluate the residual stresses holistically including lamination process with interconnect and solder material plasticity, reduced cell thickness etc. to optimize the interconnection process and topology for a more reliable solar PV technology.

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